IQ Data Framing

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Description:

This document is intended to describe the IQ data framing with a special importance on the fields of the IQ header. The IQ data framing mechanism described herein is mainly designed for coherent RTL-SDR based data acquisition systems (such as the Kerberos SDR), however it could be extended and utilized in general. According to this, the IQ header contains some special fields which are required for the basic operation of these systems

The first section introduces the structure of the IQ data frame.

The second section describes the fields of the IQ header and briefly discuss their contents and their valid values.

IQ Data Framing:

In order to properly identify the content of the downloaded and stored IQ data it is extended with a header which includes the most important status and configuration information of the data acquisition system. Figure 1. illustrates the format of the IQ data frame.

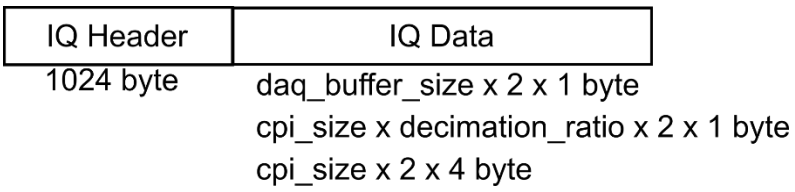

Figure 1: IQ Data frame structure

The frame has two main parts, the header and the payload sections. Internally, the length of the payload varies as it pass through the consecutive processing modules in the data acquisition and preprocessing chain. This is illustrated for the RTL-SDR based receiver in Figure 1. The first module collects daq_buffer_size iq samples and pack it to the IQ frame. Before the decimation would be completed the length of the payload is increased to cpi_size x decimation_ratio and after decimation the number of samples in the payload is reduced to cpi_size. (The actual payload size is signaled in the header.) In normal operation the transferred and the recorded IQ frames in a file has always fix cpi_size x 2 x 4 x channel_number bytes in the payload section. The data format is complex float 32. Data from the individual receiver channels are placed in blocks, one after another. However, the I and Q values of a given channel are interleaved inside the data block of the channel. This build-up is illustrated for M receiver channel in Figure 2.

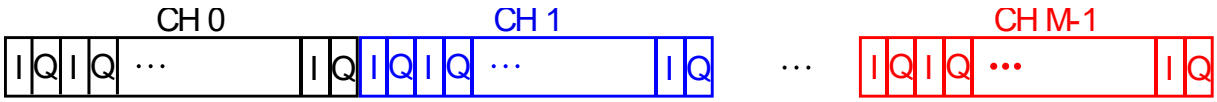

Figure 2: Structure of the payload section of the IQ data frame

In contrast to the payload the header has fixed size. The total length of the IQ header in version 6 is 1024 byte. This header is filled by the consecutive processing blocks and finally transferred together with the useful data. On the DSP side this header can be extracted, decomposed and interpreted. In IQ sample record mode, the header is saved together with the data in a structured format.

IQ Header Fields:

The following table summarize the fields of the IQ header, including their data type, length and the corresponding modules which set its values.

Field ID	Field name	Data Type	Length	Modifier Module Name
0	Header version	integer	4 byte	Realtek DAQ
1	Frame type	integer	4 byte	Realtek DAQ
2	Hardware ID	string	16 byte	Realtek DAQ
3	Unit ID	integer	4 byte	Realtek DAQ
4	Active antenna channels	integer	4 byte	Realtek DAQ
5	Illuminator Type	integer	4 byte	Realtek DAQ
6	RF Center Frequency	integer	8 byte	Realtek DAQ
7	ADC Sampling Frequency	integer	8 byte	Realtek DAQ
8	Sampling Frequency	integer	8 byte	Decimator
9	CPI length	integer	4 byte	Decimator
10	Timestamp	integer	8 byte	Realtek DAQ
11	DAQ block index	integer	4 byte	Realtek DAQ
12	CPI index	integer	4 byte	Decimator
13	Extended Integration Counter	integer	8 byte	Realtek DAQ
14	Data Type	integer	4 byte	Decimator
15	Sample Bit Depth	integer	4 byte	Realtek DAQ , Decimator
16	ADC Overdrive Detect Flags	integer	4 byte	Realtek DAQ
17	IF gain for Channel ID 0	integer	4 byte	Realtek DAQ
18	IF gain for Channel ID 1	Integer	4 byte	Realtek DAQ
	…			
48	IF gain for Channel ID 31	integer	4 byte	Realtek DAQ
49	Delay Sync Flag	integer	4 byte	Delay Synchronizer
50	IQ Sync Flag	integer	4 byte	Delay Synchronizer
51	Sync State	integer	4 byte	Delay Synchronizer
52	Noise Source State	integer	4 byte	Realtek DAQ
	Reserved		193 x 4 byte	Realtek DAQ

Table 1: List of fields of the IQ header

Header version:

Current version number of the IQ header.

Frame type:

This field is used to identify the content of the payload.

Value	Type
0	Normal data frame
1	Dummy frame
2	Ramp
3	Calibration

Table 2: Valid values of the frame type field

In normal operation frame type 0 is used, which declares that the payload contains IQ data from the receivers. Frame type: 1 used to test the links through the full data chain. Dummy frames are processed none of the daq chain modules. The ramp payload is used to verify the continuous data transfer functionality. In case the ramp data is corrupter then it could identify potential data loss in the payload. Calibration frame type indicates that the payload contains special signal which could be used to calibrate the internal distortions of the system (Time delay, Amplitude or Phase distortions).

Hardware ID:

Name of the data acquisition hardware.

Unit ID:

Numerical identifier of the current data acquisition hardware

Active antenna channels:

Indicates the currently used channel number. A single Kerberos SDR has 4 channels. The maximum number of channels is 32.

Illuminator type:

Value	Type
0	Not defined/ Custom
1	FM
2	DVB-T
3	Noise signal

Table 3: Valid values of the illuminator type field

RF Center Frequency:

RF frequency used by the R820T chip. This value is interpreted in Hz.

ADC Sampling Frequency:

Sampling frequency used by the RTL2832U chip. This value is interpreted in Hz.

Sampling Frequency:

Sampling frequency of the IQ data after decimation. This value is interpreted in Hz.

CPI (Coherent Processing Interval) Length:

Number of IQ samples stored in the payload of IQ data frame.

Timestamp:

This field contains the Unix Epoch time of the data frame. The current value is requested from the OS right before it would be sent out from the module which interact with the hardware. According to this behavior, the exact time of the data packet may differ from the actual due to the data buffering.

DAQ block index:

Contains a counter value stepped by the data acquisition module. With the checking of this field a consecutive signal processing block could be informed about potential data losses.

CPI index:

Contains a counter value stepped by the decimator module. With the checking of this field a consecutive signal processing block could be informed about potential data losses.

Extended Integration Counter:

This field stores the amount of time elapsed since the last data acquisition. In the knowledge of this time one can concatenate two consecutive data blocks to extend the duration of the coherent integration. In continuous data streaming this value is zero.

Data Type:

Value	Type
0	Dummy
1	Raw
2	IQ
3	Pre-filtered, Decimated IQ

Table 4: Valid values of the data type field

Sample bit depth:

For IQ samples, it defines only the In phase or the Quadrature part.
(e.g. : 16 means 16 bit I, 16 bit Q)

ADC Overdrive detect flags:

This flag array can be used to indicate that the ADC has been overdriven. It can be used for maximum 32 channels.
(e.g.: 0x00000003 : Means that the first and the third channels are overdriven.)

IF gain for Channel ID X:

Gain of the X-th receiver channel.

In RTL-SDR based receiver the valid values are the following:
0, 9, 14, 27, 37, 77, 87, 125, 144, 157, 166, 197, 207, 229, 254, 280, 297, 328, 338, 364, 372, 386, 402, 421, 434, 439, 445, 480, 496. To get the real gain value divide the field value by 10.
(e.g.: 87 means 8.7 dB gain)

Delay Sync Flag:

This flag array can be used to indicate that the receiver channels are out of sync in the sample level. In case this flag is 1, all the channels are synchronized, there is no sample misalignment. If it is 0 it may indicate that the channels are misaligned.

The sync state is determined from the dynamic range of the correlation peak at zero offset. In calibration tracking mode, due to the fluctuation of the ambiguity function of the used IoO this peak can fall below the used threshold and the system may incorrectly indicate sync loss. If this happens, the delay sync flag is deasserted, but only for one or two records. If the Delay Sync flag goes to zero for multiple records, the system has lost the synced state and issues a new calibration procedure. After it has been finished this flag is asserted again.

IQ Sync Flag:

This flag indicates the state of the IQ calibration. When cal_track_mode is set to 0, this flag is set after the initial calibration has been completed. Since we no longer check the current state of the IQ calibration, this flag remains true hereinafter. In case continuous calibration tracking is selected (cal_track_mode=1), this flag is updated continuously and thus reflects the actual state of the calibration from frame to frame. When burst calibration tracking is selected (cal_track_mode=2), this flag is updated regularly when calibration frames pass through the data chain (The switching between normal and calibration frames is controlled by the HC FSM).

Sync State:

Indicates the actual state of the Delay Synchronizer Finite State Machine.

Value	FSM State
0	Default value
1	INIT
2	SAMPLE CAL
3	SYNC WAIT
4	IQ CAL
5	TRACK LOCK
6	TRACK

Table 5: Valid values of the sync state field

The FSM of the HC module utilize the information encoded in this flag to control the calibration modes.

Noise Source State:

This flag is asserted when the internal noise of the data acquisition system is enabled. Otherwise it has zero value.

Reserved:

Bytes reserved for later use.